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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/629,279	NORMAN ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07292003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 are pending in the current application and have been examined.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 07/29/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner. However, the Lakhani reference is not being considered by the examiner because the serial number 09/223,08 is incomplete. Correction is required.

Drawings

3. **Figures 1, 2 and 4** are objected to because descriptive labels other than numerical are needed. See 37 CFR 1.84(o).

Figure 3 is objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: AND gates 202, 212 and 216 are missing as per specification on pages 10-11.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as

either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-4 and 6-12 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 11, 14, 15, 18- 21 of U.S. Patent No. 6,601,191. Although the conflicting claims are not identical, they are not patentably distinct from each other. The reasons for obviousness and the claim map are as follows:

Application: 10/629279	Patent No. 6,601,191
Claim 1: An over-programming detector comprising: • a first logic gate for detecting a first one of the sequential data states in data intended to be written to the array; • a second logic gate for detecting a second one of the sequential data states in data intended to be written to the array, • a third logic gate for detecting a third one of the sequential data states in data intended to be written to the array, and • a fourth logic gate for receiving data written to the array It would be obvious to one skilled in the art at the time the invention was made that the fourth logic gate would be coupled to a buffer because buffers are used in the art	Claims 11: An over-programming detector comprising: • first logic gate for detecting a first one of the sequential data states; • a second logic gate for detecting a second one of the sequential data states; • a third logic gate for detecting a third one of the sequential data states; and • a fourth logic gate coupled to the buffer.

to drive data into a device.	
Claim 2: • each logic gate is an AND gate	Claim 14: • each logic gate is an AND gate
Claims 3 and 6: An over-programming detector comprising: • a first logic gate for detecting a first one of the sequential data states in data intended to be written to the array, • a second logic gate for detecting a second one of the sequential data states in data intended to be written to the array, • a third logic gate for detecting a third one of the sequential data states in data intended to be written to the array, • a fourth logic gate coupled to the buffer and an output of the first logic gate for detecting a first over-programmed condition,	Claim 15: An over-programming detector comprising: • a first logic gate coupled to the data buffer for detecting a first one of the sequential data states; • a second logic gate coupled to the data buffer for detecting a second one of the sequential data states; • a third logic gate coupled to the data buffer for detecting a third one of the sequential data states; and • a fourth logic gate coupled to the buffer and an output of the first logic gate for detecting a first over-programmed condition;

• a fifth logic gate coupled to the buffer and an output of the second logic gate for detecting a second over-programmed condition; and • a sixth logic gate coupled to the buffer and an output of the third logic gate for detecting a third over-programmed condition.	• a fifth logic gate coupled to the buffer and an output of the second logic gate for detecting a second over-programmed condition; and • a sixth logic gate coupled to the buffer and an output of the third logic gate for detecting a third over-programmed condition.
Claims 4: • each logic gate is an AND gate	Claims 18: • each logic gate is an AND gate
Claims 6-8: An over-programming detector comprising: • a first logic gate (AND gate, claim 7) for detecting a first one of the sequential data states in data intended to be written to the array, • a second logic gate (AND gate, claim 7) for detecting a second one of the sequential data states in data intended to be written to the array, • a third logic gate (AND gate, claim	Claim 19: An over-programming detector comprising: • a first AND gate coupled to the data buffer for detecting a first one of the sequential data states; • a second AND gate coupled to the data buffer for detecting a second one of the sequential data states; • a third AND gate coupled to the

7) for detecting a third one of the sequential data states in data intended to be written to the array,	data buffer for detecting a third one of the sequential data states; and
• a fourth logic gate (AND gate, claim 7) coupled to the buffer and an output of the first logic gate for detecting a first over-programmed condition,	• a fourth AND gate coupled to the buffer, an enable input, and an output of the first AND gate for detecting a first over-programmed condition;
• a fifth logic gate (AND gate, claim 7) coupled to the buffer and an output of the second logic gate for detecting a second over-programmed condition; and	• a fifth AND gate coupled to the buffer, the enable input, and an output of the second AND gate for detecting a second over-programmed condition;
• a sixth logic gate (AND gate, claim 7) coupled to the buffer and an output of the third logic gate for detecting a third over-programmed condition.	• a sixth AND gate coupled to the buffer, the enable input, and an output of the third AND gate for detecting a third over-programmed condition; and
Claim 8:	
• a seventh logic gate coupled to respective outputs of the fourth,	• an OR-gate coupled to respective outputs of the fourth, fifth, and sixth

fifth, and sixth logic gates.	AND gates.
Claims 9 and 12: a multistate memory system comprising: • a buffer for coupling to the array of multistate memory cells; • an array of multistate memory cells, with each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states, • a memory programming coupled to the buffer for programming each of the multistate memory cells to a desired one of the sequential data states; and • at least one over-programming condition detector coupled to the	Claim 19: A control logic module for a multistate memory system, comprising: • a buffer for coupling to an array of multistate memory cells, • with each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states; • a data buffer for storing data intended to be programmed into the array of multistate memory cells; • a memory programming module coupled to the buffer for programming each of the multistate memory cells to a desired one of the sequential data states; and • at least one over-programming condition detector coupled to the

memory programming module for generating an over-programmed signal representative of one or more of the memory cells having been erroneously programmed to one of the sequential data states which is subsequent to the desired one of the sequential data states, wherein the over-programming condition detector comprises: • a first logic gate (AND gate, claim 12) for detecting a first one of the sequential data states, • a second logic gate (AND gate, claim 12)for detecting a second one of the sequential data states, • a third logic gate (AND gate, claim 12)for detecting a third one of the sequential data states and • a fourth logic gate (AND gate, claim 12) coupled to the buffer.	buffer and the data buffer for generating an over-programmed signal representative of one or more of the memory cells having been erroneously programmed to one of the sequential data states which is subsequent to the desired one of the sequential data states, wherein the over-programming condition detector comprises: • a first AND gate coupled to the data buffer for detecting a first one of the sequential data states; • a second AND gate coupled to the data buffer for detecting a second one of the sequential data states; • a third AND gate coupled to the data buffer for detecting a third one of the sequential data states; and • a fourth AND gate coupled to the buffer, an enable input, and an

	output of the first AND gate for detecting a first over-programmed condition; • a fifth AND gate coupled to the buffer, the enable input, and an output of the second AND gate for detecting a second over-programmed condition; • a sixth AND gate coupled to the buffer, the enable input, and an output of the third AND gate for detecting a third over-programmed condition; and • an OR-gate coupled to respective outputs of the fourth, fifth, and sixth AND gates.
Claim 10: • the memory programming module is configured to program each of the multistate memory cells to a desired state of at least four sequential data	Claim 20: • the memory programming module is configured to program each of the multistate memory cells to a desired state of at least four sequential data

states.	states.
Claim 11: • the memory programming module is configured to program multistate flash memory cells	Claim 21: • the memory programming module is configured to program multistate flash memory cells.

Claim Objections

4. **Claims 1, 3, 6 and 9** are objected to for the following problems:

a.) the phrase "the sequential data states" should be changes to "the at least four sequential data states.

b.) the phrase "data intended to be written" should be changed to "data to be written".

5. **Claim 2** is objected to because as disclosed by the specification and Figure 3 "the fourth logic gate is not an AND gate but a NAND gate. This claim should be amended to reflect this.

6. **Claim 10** is objected to because the limitation "a desired state of at least four sequential data states" should be "said desired state of said at least four sequential data states".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1, 2, 9–12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

This claim is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: There is no connection between the preamble and the body of the claim. The preamble recites "an over-programming condition detector", however, there is no element recited that performs the over-programming detecting.

Clarification and correction is required.

Claim 9:

This claim is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: The claim recites "an over-programming condition detector"...."for generating an over-programmed signal", however, there is no element recited that generates the over-programmed signal. Clarification and correction is required.

Claims 2, 10-12:

These claims are also rejected because they depend on a base rejected claim and have the same problems as being incomplete for omitting essential elements.

Claims 3 and 6:

These claims recite the limitation "the buffer". There is insufficient antecedent basis for this limitation in the claim.

These claims are also rejected as being indefinite because it is not clear in the written description or the figures how "the buffer" is connected to the fourth-sixth logic gates (interpreted as AND gates 202, 212 and 216, Fig. 3). No buffer is connected to these logic gates. The only buffer connected to the over-programming circuit 106 of Fig. 3 is buffer 100 of Fig. 2 for supplying the initial data bits IA and IB to AND gates 200, 210 and 214. Clarification and correction is required.

Claims 4-5 and 7-8:

These claims are also rejected because they depend on a base rejected claim and have the same problems for insufficient antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by **Endoh et al.** (US-5602789), hereinafter Endoh.

Claim 1:

Endoh teaches an over-programming condition detector (**word line controller 14, Fig. 7, By checking the four data items stored in the data latch circuit using the detection circuit, it is determined whether multi-level data is written to each memory cell correctly, insufficiently, or excessively, Fig. 25, col. 29, ll. 10-40**) for use with an array of multistate memory cells , each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states (**each of the memory cells stores three or more multi-level data "i" (i=0, 1, 2, 3, . . . , n-2, n-1: n ≥ 3)**, col. 5, l. 32-37; **Fig. 20A shows a selected one memory cell 82 from which n-valued multi-level data is read out**, col. 27, l. 64 to col. 28, l. 6, col. 28, ll. 51-61, Fig. 24A-C), the detector comprising: a first logic gate (**Fig. 7, erase control circuit 110B**, col. 14, l.61 to col. 15, l. 8) for detecting a first one of the sequential data states in data intended to be written to the array, a second logic gate (**Fig. 7, first verify circuit 106 detects insufficient write condition**) for detecting a second one of the sequential data states in data intended to be written to the array, a third logic gate (**Fig. 7, second verify circuit 108 detects excess write condition**) for detecting a third one of the sequential data states in data intended to be written to the array, and a fourth logic gate (**Fig. 7, read control circuit 110B**, col. 14, l.61 to col. 15, l. 8) for receiving data written to the array. (Col. 13, l. 45 to col. 14, l. 15).

Claims 3 and 6:

Endoh teaches an over-programming condition detector (**word line controller 14, Fig. 7, By checking the four data items stored in the data latch circuit using**

the detection circuit, it is determined whether multi-level data is written to each memory cell correctly, insufficiently, or excessively, Fig. 25, col. 29, ll. 10-40) for use with an array of multistate memory cells, each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states (**each of the memory cells stores three or more multi-level data "i" (i=0, 1, 2, 3, . . . , n-2, n-1: n ≥ 3)**, col. 5, l. 32-37; **Fig. 20A shows a selected one memory cell 82 from which n-valued multi-level data is read out**, col. 27, l. 64 to col. 28, l. 6, col. 28, ll. 51-61, Fig. 24A-C), the detector comprising: a first logic gate (**Fig. 7, erase control circuit 110B**, col. 14, l.61 to col. 15, l. 8) for detecting a first one of the sequential data states in data intended to be written to the array, a second logic gate (**Fig. 7, first verify circuit 106 detects insufficient write condition**) for detecting a second one of the sequential data states in data intended to be written to the array, a third logic gate (**Fig. 7, second verify circuit 108 detects excess write condition**) for detecting a third one of the sequential data states in data intended to be written to the array.

In light of the 35 U.S.C. 112, second paragraph rejections for "the buffer" missing from theses claims the Examiner understands **Endoh** as teaching a fourth logic gate (**Node N3 logically is a wired AND**) coupled to the buffer and an output of the first logic gate for detecting a first over-programmed condition, a fifth logic gate (**Node N2 logically is a wired AND**) coupled to the buffer and an output of the second logic gate for detecting a second over-programmed condition; and a sixth logic gate (**Node N4**

logically is a wired AND) coupled to the buffer and an output of the third logic gate for detecting a third over-programmed condition. (Col. 13, l. 45 to col. 14, l. 15).

Claims 5 and 8:

Endoh teaches a seventh logic gate (**Node N5 logically is a wired AND**) coupled to respective outputs of the fourth (**Node N3**), fifth (**Node N2**), and sixth (**Node N4**) logic gates.

Claim 9:

Endoh teaches a multistate memory system comprising: an array of multistate memory cells, with each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states (**each of the memory cells stores three or more multi-level data "i" (i=0, 1, 2, 3, . . . , n-2, n-1: n ≥ 3)**, col. 5, l. 32-37; **Fig. 20A shows a selected one memory cell 82 from which n-valued multi-level data is read out**, col. 27, l. 64 to col. 28, l. 6, col. 28, ll. 51-61, Fig. 24A-C), a buffer (**Fig. 1, data buffer 34**) for coupling to the array of multistate memory cells; a memory programming module (**Fig. 7, Word line controller 14, high-voltage supply circuit 102 and midlevel voltage supply circuit 104**, col. 13, l. 56 to col. 14, l. 15) coupled to the buffer for programming each of the multistate memory cells to a desired one of the sequential data states; and at least one over-programming condition detector (**word line controller 14, Fig. 7, By checking the four data items stored in the data latch circuit using the detection circuit, it is determined whether multi-level data is written to each memory cell correctly, insufficiently, or excessively, Fig. 25, col. 29, ll. 10-40**) coupled to the memory programming module

for generating an over-programmed signal representative of one or more of the memory cells having been erroneously programmed to one of the sequential data states which is subsequent to the desired one of the sequential data states (**each of the memory cells stores three or more multi-level data "i" (i=0, 1, 2, 3, . . . , n-2, n-1: n ≥ 3)**, col. 5, l. 32-37; **Fig. 20A shows a selected one memory cell 82 from which n-valued multi-level data is read out**, col. 27, l. 64 to col. 28, l. 6, col. 28, ll. 51-61, Fig. 24A-C), wherein the over-programming condition detector comprises: a first logic gate (**Fig. 7, erase control circuit 110B**, col. 14, l.61 to col. 15, l. 8) for detecting a first one of the sequential data states, a second logic gate (**Fig. 7, first verify circuit 106 detects insufficient write condition**) for detecting a second one of the sequential data states, a third logic gate (**Fig. 7, second verify circuit 108 detects excess write condition**) for detecting a third one of the sequential data states and a fourth logic gate (**Fig. 7, read control circuit 110B**, col. 14, l.61 to col. 15, l. 8) coupled to the buffer. (Col. 13, l. 45 to col. 14, l. 15).

Claim 10:

Endoh teaches the memory programming module (**Fig. 7, Word line controller 14, high-voltage supply circuit 102 and midlevel voltage supply circuit 104**, col. 13, l. 56 to col. 14, l. 15) is configured to program each of the multistate memory cells to a desired state of at least four sequential data states. (The four states of programming are shown in col. 28, l. 51 to col. 29, l. 40).

Claim 11:

Endoh teaches the memory programming module is configured to program multistate flash memory cells (**The EEPROM of this type is generally called a "NAND-cell type EEPROM" or "NAND type EEPROM,"**). (See Background of Invention).

Claims 2, 4, 7 and 12:

Endoh teaches each logic gate is an AND gate in that the **erase control circuit 110B** (first logic gate) has two inverted inputs from G5 and G6 going into NAND G7 (an AND gate), the **first verify circuit 106** (second logic gate) has NAND G4 and inverter I1, and the **second verify circuit 108** (third logic gate) has NAND G5 and inverter I2. The fourth, fifth and sixth logioc gates are the wired AND nodes as per the rejection of claims 3 and 6.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JACQUES H. LOUIS JACQUES can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr.
Examiner
Art Unit 2117

2/8/08

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